AMENDMENTS TO THE CLAIMS

1. (Currently amended) A semiconductor device in which one or more semiconductor chips have been mounted onto front faces of one or more substrates having front faces, rear faces and one or more side faces connecting said front faces and rear faces, said substrates incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins, wherein:

one or more electrically conductive patterns for shielding is or are formed at said one or more ~~end~~ side faces ~~at the top~~ of at least one of the substrate or substrates.

2. (Original) A semiconductor device according to claim 1 wherein:

at least one of the electrically conductive pattern or patterns is at least one copper foil pattern.

3. (Original) A semiconductor device according to claim 2 wherein:

at least one plating having good shielding characteristics is applied over at least one of the copper foil pattern or patterns.

4. (Original) A semiconductor device according to claim 3 wherein:

at least one of the plating or platings is gold plating.

4. (Previously presented) A semiconductor device according to claim 2 wherein:

one or more shield cases is or are attached over at least one of the electrically conductive pattern or patterns by way of one or more intervening electrically conductive adhesives.

6. (Original) A semiconductor device according to claim 5 wherein:

at least one of the shield case or cases is gold-plated.

7. (Previously presented) A semiconductor device according to claim 4 wherein:

one or more shield cases is or are attached over at least one of the electrically conductive pattern or patterns by way of one or more intervening silver pastes.

8. (Currently amended) A semiconductor device in which one or more semiconductor chips have been mounted onto front faces of one or more substrates having front faces, rear faces and one or more side faces connecting said front faces and rear faces, said substrate incorporating patterned wiring and the entirety or entireties of the one or more semiconductor chips has or have been sealed with one or more resins, wherein:

one or more electrically conductive patterns is or are formed at one or more ~~end~~ side faces ~~at the bottom~~ of at least one of the substrate or substrates; and

~~at least as many terminal or~~ one or more terminals ~~of such number, size, and shape as is or are sufficient~~ required for connection ~~to~~ between the patterned wiring and at least one of the electrically conductive pattern or patterns is or are formed by using one or more dies to blank out and shape at least one region at or in the vicinity of at least one of the electrically conductive pattern or patterns.

9. (Original) A semiconductor device according to claim 8 wherein:

at least one of the terminal or terminals is formed so as to at least partially protrude to the exterior and so as to have at least one more or less rectangular cross-section.

10. (Previously presented) A semiconductor device according to claim 8 wherein:

at least one gold plating is applied to at least one end face of at least one of the terminal or terminals.

Claims 11 and 12 (Cancelled).

13. (Previously presented) A semiconductor device according claim 3 wherein:

one or more shield cases is or are attached over at least one of the electrically conductive pattern or patterns by way of one or more intervening electrically conductive adhesives.

14. (Previously presented) A semiconductor device according to claim 4 wherein:

one or more shield cases is or are attached over at least one of the electrically conductive pattern or patterns by way of one or more intervening electrically conductive adhesives.

15. (Previously presented) A semiconductor device according to claim 6 wherein:

one or more shield cases is or are attached over at least one of the electrically conductive pattern or patterns by way of one or more intervening silver pastes.

Claims 16-20 (Cancelled).

21. (New) A semiconductor device comprising:

a substrate incorporating patterned wiring and having a first surface, a second surface generally parallel to said first surface, and at least one peripheral edge surface connecting said first surface and said second surface;

one or more semiconductor chips mounted on said first surface and sealed with one or more resins; and

an electrically conductive shielding pattern at at least a portion of said at least one peripheral edge surface.

22. (New) A semiconductor device according to claim 21, wherein said at least one peripheral edge comprise a first peripheral edge having terminals for connecting said semiconductor device to a circuit board and a second edge spaced from said first edge, wherein said electrically conductive shielding pattern covers said second edge.

23. (New) A semiconductor device according to claim 21 wherein said at least one peripheral edge comprises a first edge, a second edge parallel to said first edge and third and

fourth edges connecting said first and second edges, wherein said electrically conductive shielding pattern is formed on one of said first, second, third and fourth edges.